

Sink/Source DDR Termination Regulator

DESCRIPTION

The EUP7998 is a high performance linear regulator designed to provide power for termination of a DDR memory bus. It significantly reduces parts count, board space and overall system cost over previous switching solutions.

The EUP7998 maintains a fast transient response using only 20 μ F or 30 μ F output capacitance. The EUP7998 supports a remote sensing function and all power requirements for DDR, DDR2, DDR3 and Low Power DDR3/DDR4 VTT bus termination.

The EUP7998 provides current and thermal limits to prevent damage to the linear regulator. Additionally, The EUP7998 generates an open-drain PGOOD signal to monitor the output regulation. An active high enable pin EN can pull VTT low, but REFOUT will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

The EUP7998 is available in the 3mm \times 3mm TDFN-10 package.

FEATURES

- VLDOIN Input Voltage Range: 1.1V to 3.5V
- VIN Input Voltage Range: 2.375V to 5.5V
- Typically 3 \times 10 μ F MLCCs stable for DDR
- Fast Load-Transient Response
- \pm 10mA Buffered Reference (REFOUT)
- Meet DDR, DDR2 JEDEC Specifications. Supports DDR3 and Low-Power DDR3/DDR4 VTT Applications
- Power-Good Window Comparator
- With Soft Start, UVLO and OCP
- Thermal Shutdown
- Available in 10-Pin 3mm \times 3mm TDFN package
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

APPLICATIONS

- Notebook/Desktop/Server
- DDR Memory Termination
- Telecom/Datacom, GSM Base Station, LCD-TV/PDP-TV, Copier/Printer, Set-Top Box

Typical Application Circuit

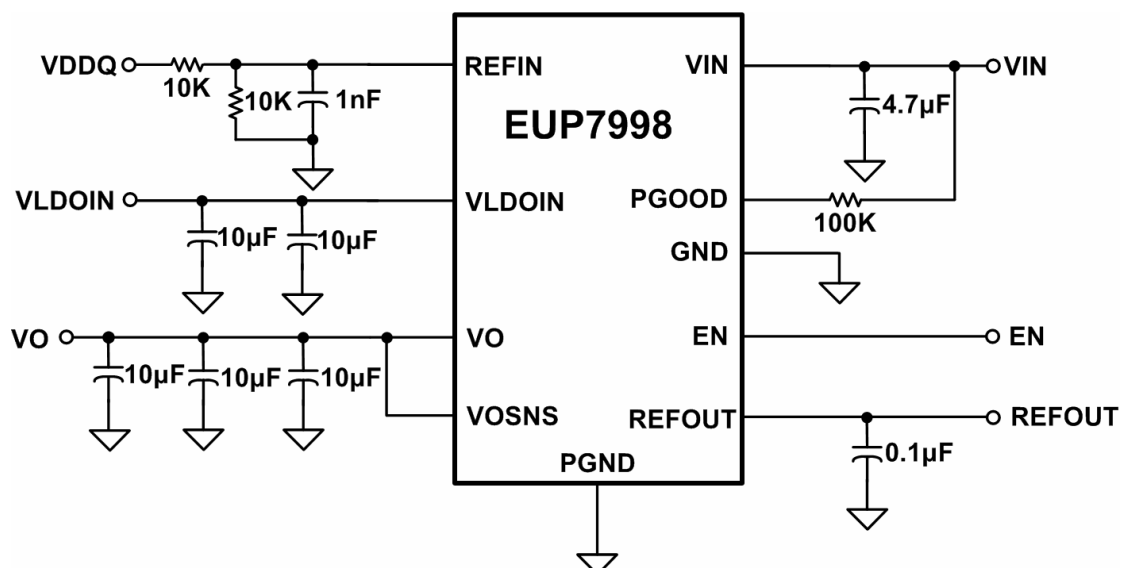


Figure 1.